AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-7. (cancelled)

8. (previously presented) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor with the interlayer dielectric layer being in direct contact with a component of the non-volatile memory transistor,

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer includes a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, and a second oxide film provided on and in direct contact with the layer containing nitride.

9. (previously presented) A semiconductor device according to claim 8, wherein the first oxide film has a thickness of 10 – 80nm.

10. (previously presented) A semiconductor device according to claim 8, wherein the first oxide film has a thickness of 30 – 70nm.

11. (previously presented) A semiconductor device according to claim 8, wherein the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

12-21. (cancelled)

22. (previously presented) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor,

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer comprises a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, and a second oxide film provided on and in direct contact with the layer containing nitride.

23. (previously presented) A semiconductor device according to Claim 22, wherein the first oxide film has a thickness of 10-80nm.

24. (previously presented) A semiconductor device according to Claim 22, wherein the first oxide film has a thickness of 30-70nm.

25. (previously presented) A semiconductor device according to Claim 22, wherein the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

26. (new) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor with the interlayer dielectric layer being in direct contact with a component of the non-volatile memory transistor; and

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer includes a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, a second oxide film provided on and in direct contact with the layer containing nitride, and the first oxide film is free of boron and phosphorus.

27. (new) A semiconductor device according to Claim 26, wherein the first oxide film has a thickness of 10-80nm.

28. (new) A semiconductor device according to Claim 26, wherein the first oxide film has a thickness of 30-70nm.

29. (new) A semiconductor device according to Claim 26, wherein the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

30. (new) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor; and

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer comprises a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, a second oxide film provided on and in direct contact with the layer containing nitride, and the first oxide film is free of boron and phosphorus.

31. (new) A semiconductor device according to Claim 30, wherein the first oxide film has a thickness of 10-80nm.

32. (new) A semiconductor device according to Claim 30, wherein the first oxide film has a thickness of 30-70nm.

33. (new) A semiconductor device according to Claim 30, wherein the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

34. (new) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor; and

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer comprises a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, a second oxide film provided on and in direct contact with the layer containing nitride, and the first oxide film has a thickness of 30-70nm.

35. (new) A semiconductor device according to Claim 34, wherein the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

AMENDMENTS TO THE DRAWINGS

The attached "Replacement Sheets" of drawings include changes to Figure 18 to reflect that this figure is "Prior Art." The attached "Replacement Sheets," which include Figures 1-18, replace the original sheets including Figures 1-18.

Attachment: Replacement Sheets